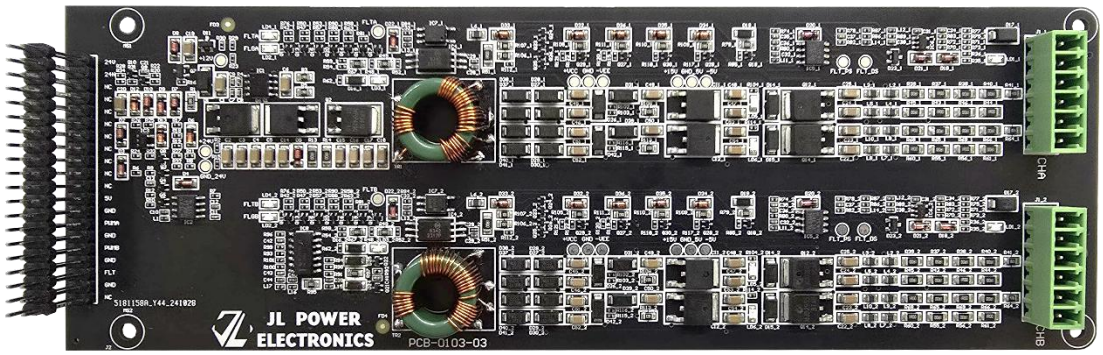
JLDRV01
Insulated Dual IGBT Gate Driver



Overview

The JLDRV01 is a dual insulated Gate Driver designed for IGBT modules up to 1200 V operating in ‘leg configuration’. Two outputs per channel are available for connecting modules in parallel.

It has open load detection and protection against output undervoltage and overvoltage, desaturation, and shoot-through with intrinsic dead time, ensuring greater reliability and robustness.

Features

- +15 V / -5.0 V output voltage for high/low output signals
- 15 A output current per channel
- 2.5 W of output power per channel
- Switching frequency up to 20 kHz

Applications

- Solar Inverters
- Motor Drivers
- Uninterruptible Power Supplies (UPS)

Technical Specification

Table 1 – Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Unit
Power Supply voltage	19.2	24	26	V
Signal Supply voltage	4.75	5	5.25	V
PWM pin input voltage	4.75	5	5.25	V
Delay time	-	250	-	ns
Common Mode Transient Immunity	20	-	-	kV/µs
Working Insulation Voltage (peak)	-	-	567	V
Maximum Insulation Voltage (1 minute)	-	-	5	kV
High Level Output Voltage	-	15	-	V
Low Level Output Voltage	-	-5	-	V
Maximum Output Current	-	-	15	A
Output Power (1)	-	-	2.5	W
Switching frequency (1)	-	-	20	kHz
Dead time	-	1.2	-	µs
Internal gate resistor (2)	-	2	-	Ω

Notes:

(1) Output power and switching frequency must be analyzed together. Maximum output power cannot be achieved by operating at maximum switching frequency.
(2) Equivalent resistance formed by the association of resistors on the gate and emitter pin for each device. The ideal gate resistance must be calculated and if necessary, an external gate resistor must be added by the user before the start of operation.

Package Outline

Units: mm

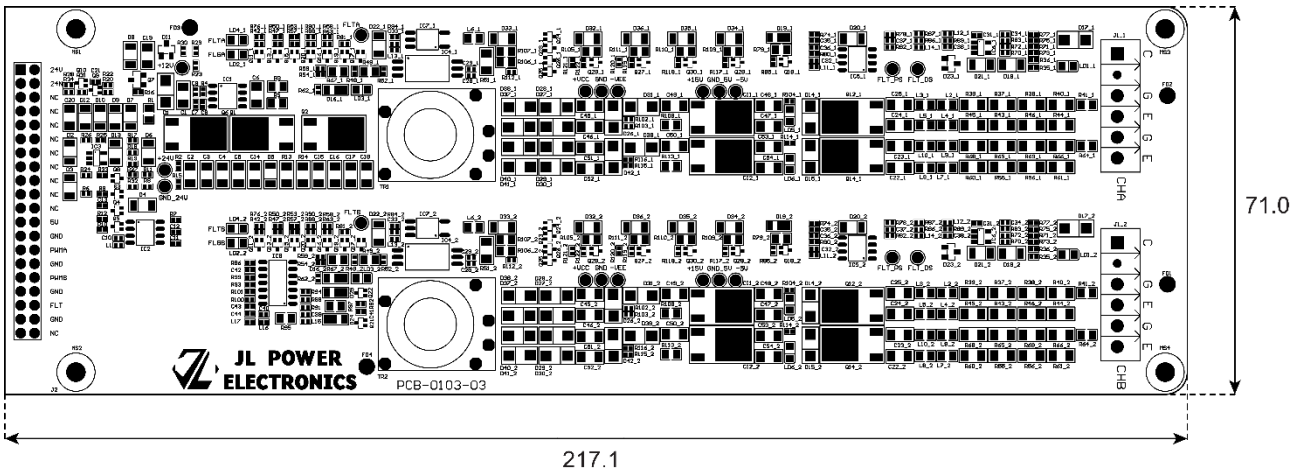


Figure 1 – Board Dimensions

All components are located on the top surface of the board.

Pin Configuration and Functions

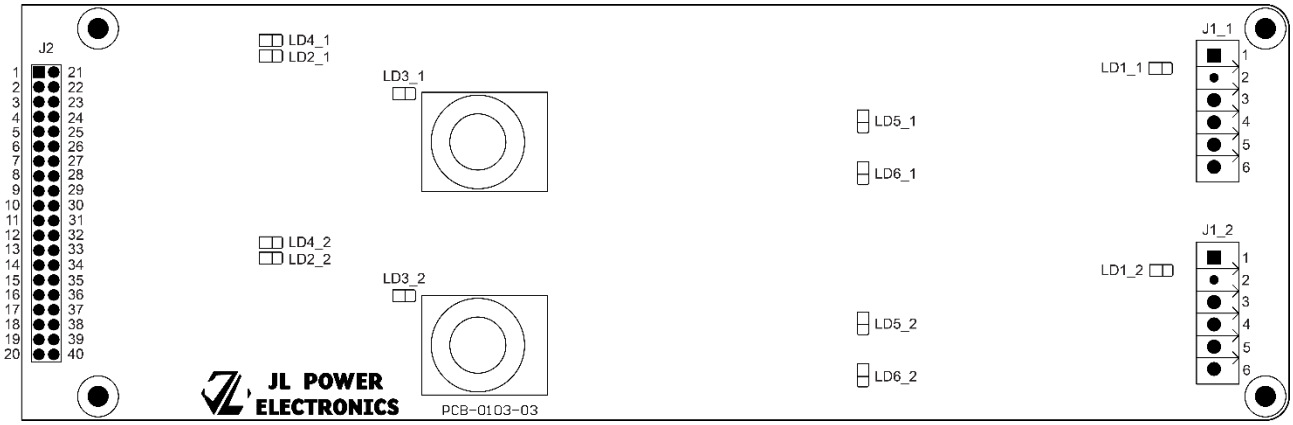


Figure 2 –Board Pin Map

Note: Components with subscription 1 (_1) refer to channel A, and with subscription 2 (_2) refer to channel B.

Table 2 – Input connector pin description (Connector J2)

Pin NO.	Designator	Description
1 / 21	24V	Power supply pin. Must be connected to +24.0 V
2 / 22	24N	Power supply reference
12 / 32	5 V	Signal supply pin. Must be connected to +5.0 V
14 / 34	PWMA	PWM input signal related to the channel A
16 / 36	PWMB	PWM input signal related to the channel B
18 / 38	FLT	Open collector fault output pin, which is driven when a PWM signal is sent while the output is open (no IGBT device is connected) or when the protection against output undervoltage, overvoltage, desaturation or shoot-through is activated
13 / 33 15 / 35 17 / 37 19 / 39	GND	Signal supply/input PWM signals reference
3-11 / 23-31 20 / 40	NC	Not Connected

Table 3 – Output connectors pin description (Connectors J1_1 and J1_2)

Pin NO.	Description
1	Collector
2	NC
3	Gate 1
4	Emitter 1
5	Gate 2
6	Emitter 2

Note: Each connector has two gate pins and two emitter pins for connecting modules in parallel if desired.

Table 4 – LED indicators description

Designator	Description
LD1_1 / LD1_2	Indicates the gate signal of the IGBTs of the respective channel
LD3_1 / LD3_2	Indicates the IGBTs control signals before the optocouplers
LD4_1 / LD4_2 (FLTA / FLTB)	Indicates that a PWM signal is being sent while the output is open (no IGBT device is connected) or that the protection against output undervoltage and overvoltage or desaturation or shoot-through is activated. The indication remains only during the event
LD2_1 / LD2_2 (FLGA / FLGB)	Indicates that a PWM signal has been sent while the output was open (no IGBT device was connected) or that the protection against undervoltage or overvoltage at the output or desaturation or shoot-through has been activated. The indication remains even after the event has ended and is only reset after a new PWM pulse
LD5_1 / LD5_2	Indicates whether the output high voltage power supply is working properly
LD6_1 / LD6_2	Indicates whether the output low voltage power supply is working properly

Table 5 – Operational logical truth table

PWMA	PWMB	FLT	CH A Output	CH B Output
L	L	Open-drain	L	L
H	L	Open-drain	H	L
L	H	Open-drain	L	H
H	H	Open-drain	L	L
X	X	H	L	L